UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/497,154	02/03/2000	Makoto Monoi	0039-7552-2	7156

22850 7590 03/26/2004

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
HENN, TIMOTHY J	

ART UNIT	PAPER NUMBER
2612	6

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/497,154	MONOI, MAKOTO	
	Examiner	Art Unit	
	Timothy J Henn	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 21-29* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 February 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1-3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. **It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.**

3. The spacing of the lines of the specification is such as to make reading and entry of amendments difficult. New application papers with lines double spaced on good quality paper are required.

4. The claims are objected to because the lines are crowded too closely together, making reading and entry of amendments difficult. Substitute claims with lines one and

one-half or double spaced on good quality paper are required. See 37 CFR 1.52(b).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al. (US 5,506,429).

[claim 1]

7. In regard to claim 1, note that Tanaka discloses a solid image pickup apparatus (Figure 1, Item 20) comprising: a pixel string in which a plurality of photoelectric converting sections corresponding to pixels are arranged in one string (Figure 1, Items P1 and P5); a CCD register (Figure 1, Item 24), adjacently arranged to said pixel string, for successively transferring, in a predetermined direction, signal charges photoelectrically converted in the respective photoelectric converting sections (Column 4, Lines 48-50); a wiring layer (Figure 2, Item 34) formed above said CCD register and its periphery via an insulating layer (Figure 2, Item 38); and a contact formed in a strip shape along electric charge transfer direction of said CCD register and connected to said wiring layer (Figure 2, Item C1).

[claim 2]

8. In regard to claim 2, note that Tanaka discloses a solid image pickup apparatus (Figure 1, Item 20) comprising: a pixel string in which a plurality of photoelectric converting sections corresponding to pixels are arranged in one string (Figure 1, Items P1 and P5); a CCD register (Figure 1, Item 24), adjacently arranged to said pixel string, for successively transferring, in a predetermined direction, signal charges photoelectrically converted in the respective photoelectric converting sections (Column 4, Lines 48-50); a transfer electrode for supplying a voltage for transferring to said CCD register (Figure 2, electrode below C1); n (n is an integer of two or more) pieces of wiring layers (Figure 2, Items 34 and 36) formed in lamellar shape above said transfer electrode and its periphery via an insulating layer (Figure 2, Items 38 and 39); and a contact formed in a strip shape along electric charge transfer direction of said CCD register to at least one location between the transfer electrode and the wiring layer (Figure 2, Item C1) and between two wiring layers vertically adjacent to each other (Figure 2, Item C2) via said insulating layer.

[claim 3]

9. In regard to claim 3, note that Tanaka discloses a solid image pickup apparatus (Figure 1, Item 20) comprising: a pixel string in which a plurality of photoelectric converting sections corresponding to pixels are arranged in one string (Figure 1, Items P1 and P5); a CCD register (Figure 1, Item 24), adjacently arranged to said pixel string, for successively transferring, in a predetermined direction, signal charges photoelectrically converted in the respective photoelectric converting sections (Column 4, Lines 48-50); n (n is an integer of two or more) pieces of wiring layers (Figure 2,

Items 34 and 36) formed in lamellar shape above said CCD register and its periphery via an insulating layer (Figure 2, Items 38 and 39); and a contact formed in a strip shape along electric charge transfer direction of said CCD register to at least one location between the transfer electrode and the wiring layer (Figure 2, Item C1) and between two wiring layers vertically adjacent to each other (Figure 2, Item C2) via said insulating layer.

10. Claims 1, 4 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by the applicants admitted prior art.

[claim 1]

11. In regard to claim 1, note that the applicants admitted prior art discloses a solid state image pickup apparatus (Figure 1) comprising: a pixel string in which a plurality of photoelectric converting sections corresponding to pixels are arranged in one string (Figure 1, Item 1b); a CCD register (Figure 1, Item 3b), adjacently arranged to said pixel string, for successively transferring, in a predetermined direction, signal charges photoelectrically converted in the respective photoelectric converting sections (Page 1, Lines 30-36); a wiring layer (Figure 3, Items 8 and 80) formed above said CCD register and its periphery via an insulating layer; and a contact formed in a strip shape along electric charge transfer direction of said CCD register and connected to said wiring layer (Figure 2, Items 9).

[claim 4]

12. In regard to claim 4, note that the applicants admitted prior art discloses a solid image pickup apparatus wherein said wiring layer (Figure 3, Item 6) is disposed to apply a voltage to at least one of the transfer electrode (Figure 3, Item 31) of said CCD register, an electrode other than the electrode of said CCD register (Figure 3, Item 2b), and a semiconductor area (Figure 3, Region 11 and part of Region 12).

[claim 7]

13. In regard to claim 7, note that the applicants admitted prior art discloses a shift electrode (Figure 3, Item 2b) which is formed between said pixel string (Figure 3, Item 1b) and said CCD register (Figure 3, Item 12) and which transfers, to said CCD register, the signal charges photoelectrically converted in the respective photoelectric converting sections in said pixel string (Page 1, Lines 30-32); a shift electrode wiring layer for applying a voltage for transferring electric charge to said shift electrode (Figure 3, Item 6); and a contact which is formed into a strip shape along a direction crossing substantially at right angles to electric charge transfer direction under said shift electrode and which connects said shift electrode to said shift electrode wiring layer (Figure 2, Item 7).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 2, 3, 5, 6, 8-19 and 25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicants admitted prior art in view of Tanaka et al. (US 5,506,429).

[claim 2]

16. In regard to claim 2, note that the applicants admitted prior art discloses a solid state image pickup (Figure 1) apparatus comprising: a pixel string in which a plurality of photoelectric converting sections corresponding to pixels are arranged in one string (Figure 1, Item 1b); a CCD register (Figure 1, Item 3b), adjacently arranged to said pixel string, for successively transferring, in a predetermined direction, signal charges photoelectrically converted in the respective photoelectric converting sections (Page 1, Lines 30-36); a transfer electrode for supplying a voltage for transferring to said CCD register (Figure 3, Item 31); and a contact (Figure 2, Item 9) formed in a strip shape along electric charge transfer direction of said CCD register to at least one location between the transfer electrode and the wiring layer (Figure 3, Item 80). Therefore, it can be seen that the applicants admitted prior art lacks n (n is an integer of two or more) pieces of wiring layers formed in lamellar shape above said transfer electrode and its periphery via an insulating layer and a contact formed in a strip shape along electric charge transfer direction of said CCD register to at least one location between two wiring layers vertically adjacent to each other via said insulating layer.

17. Tanaka et al. discloses a "double-layered transfer gate" structure (Column 5, Lines 11-25) which prevents the occurrence of pulse delay and rounding of pulse wave-forms (Column 1, Lines 44-55). It would have been obvious to one of ordinary skill in

the art at the time the invention was made to combine the double-layered transfer gate structure of Tanaka et al. with the transfer electrode of the applicants admitted prior art to prevent the occurrence of pulse delay and rounding of pulse wave-forms when driving the solid state image pickup apparatus.

[claim 3]

18. In regard to claim 2, note that the applicants admitted prior art discloses a solid state image pickup (Figure 1) apparatus comprising: a pixel string in which a plurality of photoelectric converting sections corresponding to pixels are arranged in one string (Figure 1, Item 1b); a CCD register (Figure 1, Item 3b), adjacently arranged to said pixel string, for successively transferring, in a predetermined direction, signal charges photoelectrically converted in the respective photoelectric converting sections (Page 1, Lines 30-36); Therefore, it can be seen that the applicants admitted prior art lacks n (n is an integer of two or more) pieces of wiring layers formed in lamellar shape above said CCD register and its periphery via an insulating layer and a contact formed in a strip shape along electric charge transfer direction of said CCD register to at least one location between two wiring layers vertically adjacent to each other via said insulating layer.

19. Tanaka et al. discloses a "double-layered transfer gate" structure (Column 5, Lines 11-25) which prevents the occurrence of pulse delay and rounding of pulse wave-forms (Column 1, Lines 44-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the double-layered transfer gate structure of Tanaka et al. with the transfer electrode above the CCD register of the

applicants admitted prior art to prevent the occurrence of pulse delay and rounding of pulse wave-forms when driving the solid state image pickup apparatus.

[claim 5]

20. In regard to claim 5, note that the applicants admitted prior art discloses a solid image pickup apparatus wherein said wiring layer (Figure 3, Item 6) is disposed to apply a voltage to at least one of the transfer electrode (Figure 3, Item 31) of said CCD register, an electrode other than the electrode of said CCD register (Figure 3, Item 2b), and a semiconductor area (Figure 3, Region 11 and part of Region 12).

[claim 6]

21. In regard to claim 6, note that the applicants admitted prior art discloses a solid image pickup apparatus wherein said wiring layer (Figure 3, Item 6) is disposed to apply a voltage to at least one of the transfer electrode (Figure 3, Item 31) of said CCD register, an electrode other than the electrode of said CCD register (Figure 3, Item 2b), and a semiconductor area (Figure 3, Region 11 and part of Region 12).

[claim 8]

22. In regard to claim 8, note that the applicants admitted prior art discloses a shift electrode (Figure 3, Item 2b) which is formed between said pixel string (Figure 3, Item 1b) and said CCD register (Figure 3, Item 12) and which transfers, to said CCD register, the signal charges photoelectrically converted in the respective photoelectric converting sections in said pixel string (Page 1, Lines 30-32); a shift electrode wiring layer for applying a voltage for transferring electric charge to said shift electrode (Figure 3, Item 6); and a contact which is formed into a strip shape along a direction crossing

substantially at right angles to electric charge transfer direction under said shift electrode and which connects said shift electrode to said shift electrode wiring layer (Figure 2, Item 7).

[claim 9]

23. In regard to claim 9, note that the applicants admitted prior art discloses a shift electrode (Figure 3, Item 2b) which is formed between said pixel string (Figure 3, Item 1b) and said CCD register (Figure 3, Item 12) and which transfers, to said CCD register, the signal charges photoelectrically converted in the respective photoelectric converting sections in said pixel string (Page 1, Lines 30-32); a shift electrode wiring layer for applying a voltage for transferring electric charge to said shift electrode (Figure 3, Item 6); and a contact which is formed into a strip shape along a direction crossing substantially at right angles to electric charge transfer direction under said shift electrode and which connects said shift electrode to said shift electrode wiring layer (Figure 2, Item 7).

[claim 10]

24. In regard to claim 10, note that the applicants admitted prior art lacks an upper stage wiring layer formed above said shift electrode wiring layer via the insulating layer; and a contact which is formed into the strip shape along the electric charge transfer direction of said CCD register or along a direction crossing substantially at right angles to electric charge transfer direction under said shift electrode and which connects said shift electrode wiring layer to said upper stage wiring layer.

25. Tanaka et al. discloses a "double-layered transfer gate" structure including an upper-stage wiring layer (Figure 2, Item 36) formed above the electrode wiring layer via an insulating layer (Figure 2, Item 39; Column 5, Lines 11-25) and a contact (Figure 2, Item C2) which connects the electrode wiring layer (Figure 2, Item 34) to the upper-stage wiring layer. The structure of Tanaka et al. prevents the occurrence of pulse delay and rounding of pulse wave-forms (Column 1, Lines 44-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the double-layered transfer gate structure of Tanaka et al. with the shift electrode of the applicants admitted prior art to prevent the occurrence of pulse delay and rounding of pulse wave-forms when driving the solid state image pickup apparatus.

[claim 11]

26. In regard to claim 11, note that the applicants admitted prior art lacks an upper stage wiring layer formed above said shift electrode wiring layer via the insulating layer; and a contact which is formed into the strip shape along the electric charge transfer direction of said CCD register or along a direction crossing substantially at right angles to electric charge transfer direction under said shift electrode and which connects said shift electrode wiring layer to said upper stage wiring layer.

27. Tanaka et al. discloses a "double-layered transfer gate" structure including an upper-stage wiring layer (Figure 2, Item 36) formed above the electrode wiring layer via an insulating layer (Figure 2, Item 39; Column 5, Lines 11-25) and a contact (Figure 2, Item C2) which connects the electrode wiring layer (Figure 2, Item 34) to the upper-stage wiring layer. The structure of Tanaka et al. prevents the occurrence of pulse

delay and rounding of pulse wave-forms (Column 1, Lines 44-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the double-layered transfer gate structure of Tanaka et al. with the shift electrode of the applicants admitted prior art to prevent the occurrence of pulse delay and rounding of pulse wave-forms when driving the solid state image pickup apparatus.

[claim 12]

28. In regard to claim 12, note that the applicants admitted prior art lacks an upper stage wiring layer formed above said shift electrode wiring layer via the insulating layer; and a contact which is formed into the strip shape along the electric charge transfer direction of said CCD register or along a direction crossing substantially at right angles to electric charge transfer direction under said shift electrode and which connects said shift electrode wiring layer to said upper stage wiring layer.

29. Tanaka et al. discloses a "double-layered transfer gate" structure including an upper-stage wiring layer (Figure 2, Item 36) formed above the electrode wiring layer via an insulating layer (Figure 2, Item 39; Column 5, Lines 11-25) and a contact (Figure 2, Item C2) which connects the electrode wiring layer (Figure 2, Item 34) to the upper-stage wiring layer. The structure of Tanaka et al. prevents the occurrence of pulse delay and rounding of pulse wave-forms (Column 1, Lines 44-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the double-layered transfer gate structure of Tanaka et al. with the shift electrode of the applicants admitted prior art to prevent the occurrence of pulse delay and rounding of

pulse wave-forms when driving the solid state image pickup apparatus.

[claim 13]

30. In regard to claim 13, note that the applicants admitted prior art in view of Tanaka et al. lacks a n upper-stage wiring layer that is formed of a poly-silicon layer. However, the office notes that it is well known in the art to use doped poly-silicon as a wiring material for its ability to withstand higher operational temperatures (i.e. silicon has a higher melting point that commonly used metals such as aluminum) (Official Notice). Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to use poly-silicon as the material for the upper wiring layer to allow the device to operate at higher temperatures.

[claim 14]

31. In regard to claim 14, note that the applicants admitted prior art in view of Tanaka et al. lacks a n upper-stage wiring layer that is formed of a poly-silicon layer. However, the office notes that it is well known in the art to use doped poly-silicon as a wiring material for its ability to withstand higher operational temperatures (i.e. silicon has a higher melting point that commonly used metals such as aluminum) (Official Notice). Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to use poly-silicon as the material for the upper wiring layer to allow the device to operate at higher temperatures.

[claim 15]

32. In regard to claim 15, note that the applicants admitted prior art in view of Tanaka et al. lacks a n upper-stage wiring layer that is formed of a poly-silicon layer. However,

the office notes that it is well known in the art to use doped poly-silicon as a wiring material for its ability to withstand higher operational temperatures (i.e. silicon has a higher melting point that commonly used metals such as aluminum) (Official Notice). Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to use poly-silicon as the material for the upper wiring layer to allow the device to operate at higher temperatures.

[claim 16]

33. In regard to claim 16, note that the applicants admitted prior art discloses a solid image pickup apparatus further comprising: a first wiring layer (Figure 3, Item 80) for applying a voltage for transferring electric charge to the transfer electrode (Figure 3, Item 31) of said CCD register; a first contact which is formed into a strip shape along the electric charge transfer direction of said CCD register (Figure 2, Item 3b) and which connects said transfer electrode to said first wiring layer (Figure 2, Item 9); a shift electrode (Figure 2, Item 2b) which is formed between said pixel string (Figure 2, Item 1b) and said CCD register (Figure 2, Item 3b) and which transfers the signal charges photoelectrically converted in the photoelectric converting sections in said pixel string to said CCD register; a second wiring layer (Figure 3, Item 6) for applying the voltage for transferring electric charge to said shift electrode; a second contact which is formed into a strip shape along a direction crossing substantially at right angles to electric charge transfer direction under said shift electrode and which connects said shift electrode to said second wiring layer (Figure 2, Item 7); and a shielding film (Figure 3, Item 10) formed above said third and fourth wiring layers via the insulating layer. Therefore, it

can be seen that the applicants admitted prior art lacks a third wiring layer formed above said first wiring layer via the insulating layer; a third contact which is formed into the strip shape along the electric charge transfer direction of said CCD register and which connects said first wiring layer to said third wiring layer; a fourth wiring layer formed above said second wiring layer via the insulating layer; and a fourth contact which is formed into the strip shape along a direction crossing substantially at right angles to electric charge transfer direction under said shift electrode and which connects said second wiring layer to said fourth wiring layer;

34. Tanaka et al. discloses a "double-layered transfer gate" structure including an upper-stage wiring layer (Figure 2, Item 36) formed above the electrode wiring layer via an insulating layer (Figure 2, Item 39; Column 5, Lines 11-25) and a contact (Figure 2, Item C2) which connects the electrode wiring layer (Figure 2, Item 34) to the upper-stage wiring layer. The structure of Tanaka et al. prevents the occurrence of pulse delay and rounding of pulse wave-forms (Column 1, Lines 44-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the double-layered transfer gate structure of Tanaka et al. with the shift electrode and the transfer electrode of the applicants admitted prior art to prevent the occurrence of pulse delay and rounding of pulse wave-forms when driving the solid state image pickup apparatus.

[claim 17]

35. In regard to claim 17, note that in the imager of the applicants admitted prior art, each of the wiring layers is formed so that at least two of the wiring layers does not

overlap in a vertical direction when each of the wiring layers has a gap. The office notes that the additional gate structure of Tanaka et al. would not change this feature as the additional gate wires only exist on top of the existing gate while the existing gates of the applicants admitted prior art are spaced so that there is no overlap.

[claim 18]

36. In regard to claim 17, note that in the imager of the applicants admitted prior art, each of the wiring layers is formed so that at least two of the wiring layers does not overlap in a vertical direction when each of the wiring layers has a gap. The office notes that the additional gate structure of Tanaka et al. would not change this feature as the additional gate wires only exist on top of the existing gate while the existing gates of the applicants admitted prior art are spaced so that there is no overlap.

[claim 19]

37. In regard to claim 19, note that the applicants admitted prior art discloses a solid image pickup apparatus wherein: said CCD register comprises a first transfer electrode (Figure 2, Item 31) to which a first voltage is applied, and a second transfer electrode (Figure 2, Item 32) to which a second voltage is applied, the voltage for transferring electric charge is applied to said first transfer electrode from a first wiring layer (Figure 3, Item 6), the voltage for transferring electric charge is applied to said second transfer electrode from a fifth wiring layer (Figure 3, Item 80), said first transfer electrode is connected to said first wiring layer via a first contact (Figure 2, note contact points on line 8) formed into a strip shape along the electric charge transfer direction of said CCD register, and said second transfer electrode is connected to said fifth wiring layer via a

plurality of contacts formed at predetermined intervals (Figure 2, note contact points on line 80).

[claim 25]

38. In regard to claim 25, note that the applicants admitted prior art discloses all limitations except an electric discharge gate, disposed in parallel with said pixel string, for discharging the signal charge photoelectrically converted in said photoelectric converting section; a discharge wiring layer for applying an electric discharging voltage to said electric discharge gate; and a contact which is formed into a strip shape along a direction crossing substantially at right angles to an electric discharge direction in said electric discharge gate and which connects said electric discharge gate to said discharge wiring layer. However, it is well known in the art to provide an electric charge discharge gate, wiring layer and contact as claimed to allow for the resetting of pixel photodiodes prior to the start of integration to have a consistent base level charge for each picture (Official Notice). Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a discharge gate, wire and contact as claimed to allow for resetting the array.

[claim 26]

39. In regard to claim 26, note that the applicants admitted prior art discloses all limitations except an electric discharge gate, disposed in parallel with said pixel string, for discharging the signal charge photoelectrically converted in said photoelectric converting section; a discharge wiring layer for applying an electric discharging voltage to said electric discharge gate; and a contact which is formed into a strip shape along a

direction crossing substantially at right angles to an electric discharge direction in said electric discharge gate and which connects said electric discharge gate to said discharge wiring layer. However, it is well known in the art to provide an electric charge discharge gate, wiring layer and contact as claimed to allow for the resetting of pixel photodiodes prior to the start of integration to have a consistent base level charge for each picture (Official Notice). Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a discharge gate, wire and contact as claimed to allow for resetting the array.

[claim 27]

40. In regard to claim 27, note that the applicants admitted prior art discloses a solid image pickup apparatus comprising: a shift electrode (Figure 2, Item 2b), formed between said pixel string (Figure 2, Item 1b) and said CCD register (Figure 2, Item 3b), for transferring the signal charges photoelectrically converted in the photoelectric converting sections in said pixel string to said CCD register (Page 1, Lines 30-32); and a first wiring layer (Figure 3, Item 6) for applying the voltage for transferring electric charge to said shift electrode. Therefore, it can be seen that the applicants admitted prior art lacks a second wiring layer formed above said first wiring layer via the insulating layer; and a contact which is formed into a strip shape along the electric charge transfer direction of said CCD register and which connects said first wiring layer to said second wiring layer.

41. Tanaka et al. discloses a "double-layered transfer gate" structure including an upper-stage wiring layer (Figure 2, Item 36) formed above the electrode wiring layer via

an insulating layer (Figure 2, Item 39; Column 5, Lines 11-25) and a contact (Figure 2, Item C2) which connects the electrode wiring layer (Figure 2, Item 34) to the upper-stage wiring layer. The structure of Tanaka et al. prevents the occurrence of pulse delay and rounding of pulse wave-forms (Column 1, Lines 44-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the double-layered transfer gate structure of Tanaka et al. with the shift electrode of the applicants admitted prior art to prevent the occurrence of pulse delay and rounding of pulse wave-forms when driving the solid state image pickup apparatus.

[claim 28]

42. In regard to claim 28, note that the applicants admitted prior art discloses a solid image pickup apparatus comprising: a shift electrode (Figure 2, Item 2b), formed between said pixel string (Figure 2, Item 1b) and said CCD register (Figure 2, Item 3b), for transferring the signal charges photoelectrically converted in the photoelectric converting sections in said pixel string to said CCD register (Page 1, Lines 30-32); and a first wiring layer (Figure 3, Item 6) for applying the voltage for transferring electric charge to said shift electrode. Therefore, it can be seen that the applicants admitted prior art lacks a second wiring layer formed above said first wiring layer via the insulating layer; and a contact which is formed into a strip shape along the electric charge transfer direction of said CCD register and which connects said first wiring layer to said second wiring layer.

43. Tanaka et al. discloses a "double-layered transfer gate" structure including an upper-stage wiring layer (Figure 2, Item 36) formed above the electrode wiring layer via

an insulating layer (Figure 2, Item 39; Column 5, Lines 11-25) and a contact (Figure 2, Item C2) which connects the electrode wiring layer (Figure 2, Item 34) to the upper-stage wiring layer. The structure of Tanaka et al. prevents the occurrence of pulse delay and rounding of pulse wave-forms (Column 1, Lines 44-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the double-layered transfer gate structure of Tanaka et al. with the shift electrode of the applicants admitted prior art to prevent the occurrence of pulse delay and rounding of pulse wave-forms when driving the solid state image pickup apparatus.

[claim 29]

44. In regard to claim 29, note that the applicants admitted prior art discloses a solid image pickup apparatus comprising: a shift electrode (Figure 2, Item 2b), formed between said pixel string (Figure 2, Item 1b) and said CCD register (Figure 2, Item 3b), for transferring the signal charges photoelectrically converted in the photoelectric converting sections in said pixel string to said CCD register (Page 1, Lines 30-32); and a first wiring layer (Figure 3, Item 6) for applying the voltage for transferring electric charge to said shift electrode. Therefore, it can be seen that the applicants admitted prior art lacks a second wiring layer formed above said first wiring layer via the insulating layer; and a contact which is formed into a strip shape along the electric charge transfer direction of said CCD register and which connects said first wiring layer to said second wiring layer.

45. Tanaka et al. discloses a "double-layered transfer gate" structure including an upper-stage wiring layer (Figure 2, Item 36) formed above the electrode wiring layer via

an insulating layer (Figure 2, Item 39; Column 5, Lines 11-25) and a contact (Figure 2, Item C2) which connects the electrode wiring layer (Figure 2, Item 34) to the upper-stage wiring layer. The structure of Tanaka et al. prevents the occurrence of pulse delay and rounding of pulse wave-forms (Column 1, Lines 44-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the double-layered transfer gate structure of Tanaka et al. with the shift electrode of the applicants admitted prior art to prevent the occurrence of pulse delay and rounding of pulse wave-forms when driving the solid state image pickup apparatus.

46. Claims 21, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US 5,506,429) in view of Wakayama et al. (US 5,736,756).

[claim 21]

47. In regard to claim 21, note that Tanaka et al. discloses all limitations except for a diffusion area formed adjacent to said CCD register; a substrate wiring layer for applying a predetermined voltage to a substrate through said diffusion area; and a contact which is formed into a strip shape along the electric charge transfer direction of said CCD register and which connects said diffusion area to said substrate wiring layer.

48. Wakayama et al. discloses a solid-state image sensing device with a light shielding film (Figure 1, Item 24) which contacts a diffusion area on the substrate(Figure 1) , and a potential applying means (Figure 1, Item 26) which reduces smear and dark current in the image sensor (Column 2, Lines 55-60). The office notes that the light shielding film comprises a contact (i.e. the sections running perpendicular to the

substrate) and a wiring layer (i.e. the sections running parallel to the substrate). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement a light shielding film such as that of Wakayama et al. to reduce smear and dark current in the imager of Tanaka et al.

[claim 22]

49. In regard to claim 22, note that Tanaka et al. discloses all limitations except for a diffusion area formed adjacent to said CCD register; a substrate wiring layer for applying a predetermined voltage to a substrate through said diffusion area; and a contact which is formed into a strip shape along the electric charge transfer direction of said CCD register and which connects said diffusion area to said substrate wiring layer.

50. Wakayama et al. discloses a solid-state image sensing device with a light shielding film (Figure 1, Item 24) which contacts a diffusion area on the substrate(Figure 1) , and a potential applying means (Figure 1, Item 26) which reduces smear and dark current in the image sensor (Column 2, Lines 55-60). The office notes that the light shielding film comprises a contact (i.e. the sections running perpendicular to the substrate) and a wiring layer (i.e. the sections running parallel to the substrate). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement a light shielding film such as that of Wakayama et al. to reduce smear and dark current in the imager of Tanaka et al.

[claim 23]

51. In regard to claim 23, note that Tanaka et al. discloses all limitations except for a diffusion area formed adjacent to said CCD register; a substrate wiring layer for

applying a predetermined voltage to a substrate through said diffusion area; and a contact which is formed into a strip shape along the electric charge transfer direction of said CCD register and which connects said diffusion area to said substrate wiring layer.

52. Wakayama et al. discloses a solid-state image sensing device with a light shielding film (Figure 1, Item 24) which contacts a diffusion area on the substrate(Figure 1) , and a potential applying means (Figure 1, Item 26) which reduces smear and dark current in the image sensor (Column 2, Lines 55-60). The office notes that the light shielding film comprises a contact (i.e. the sections running perpendicular to the substrate) and a wiring layer (i.e. the sections running parallel to the substrate). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement a light shielding film such as that of Wakayama et al. to reduce smear and dark current in the imager of Tanaka et al.

53. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over the applicants admitted prior art in view of Wakayama et al. (US 5,736,756).

[claim 21]

54. In regard to claim 21, note that the applicants admitted prior art discloses all limitations except for a diffusion area formed adjacent to said CCD register; a substrate wiring layer for applying a predetermined voltage to a substrate through said diffusion area; and a contact which is formed into a strip shape along the electric charge transfer direction of said CCD register and which connects said diffusion area to said substrate wiring layer.

Wakayama et al. discloses a solid-state image sensing device with a light shielding film (Figure 1, Item 24) which contacts a diffusion area on the substrate(Figure 1) , and a potential applying means (Figure 1, Item 26) which reduces smear and dark current in the image sensor (Column 2, Lines 55-60). The office notes that the light shielding film comprises a contact (i.e. the sections running perpendicular to the substrate) and a wiring layer (i.e. the sections running parallel to the substrate). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement a light shielding film such as that of Wakayama et al. to reduce smear and dark current in the imager of the applicants admitted prior art.

55. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicants admitted prior art in view of Tanaka et al. (US 5,506,429) as applied to claims 2 and 3 above, and further in view of Wakayama et al. (US 5,736,756).

[claim 22]

56. In regard to claim 22, note that the applicants admitted prior art in view of Tanaka et al. discloses all limitations except for a diffusion area formed adjacent to said CCD register; a substrate wiring layer for applying a predetermined voltage to a substrate through said diffusion area; and a contact which is formed into a strip shape along the electric charge transfer direction of said CCD register and which connects said diffusion area to said substrate wiring layer.

57. Wakayama et al. discloses a solid-state image sensing device with a light shielding film (Figure 1, Item 24) which contacts a diffusion area on the substrate(Figure

1) , and a potential applying means (Figure 1, Item 26) which reduces smear and dark current in the image sensor (Column 2, Lines 55-60). The office notes that the light shielding film comprises a contact (i.e. the sections running perpendicular to the substrate) and a wiring layer (i.e. the sections running parallel to the substrate). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement a light shielding film such as that of Wakayama et al. to reduce smear and dark current in the imager of the applicants admitted prior art in view of Tanaka et al.

[claim 23]

58. In regard to claim 23, note that the applicants admitted prior art in view of Tanaka et al. discloses all limitations except for a diffusion area formed adjacent to said CCD register; a substrate wiring layer for applying a predetermined voltage to a substrate through said diffusion area; and a contact which is formed into a strip shape along the electric charge transfer direction of said CCD register and which connects said diffusion area to said substrate wiring layer.

59. Wakayama et al. discloses a solid-state image sensing device with a light shielding film (Figure 1, Item 24) which contacts a diffusion area on the substrate(Figure 1) , and a potential applying means (Figure 1, Item 26) which reduces smear and dark current in the image sensor (Column 2, Lines 55-60). The office notes that the light shielding film comprises a contact (i.e. the sections running perpendicular to the substrate) and a wiring layer (i.e. the sections running parallel to the substrate). It would have been obvious to one of ordinary skill in the art at the time the invention was

made to implement a light shielding film such as that of Wakayama et al. to reduce smear and dark current in the imager of the applicants admitted prior art in view of Tanaka et al.

60. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over the applicants admitted prior art.

[claim 24]

61. In regard to claim 24, note that the applicants admitted prior art discloses all limitations except an electric discharge gate, disposed in parallel with said pixel string, for discharging the signal charge photoelectrically converted in said photoelectric converting section; a discharge wiring layer for applying an electric discharging voltage to said electric discharge gate; and a contact which is formed into a strip shape along a direction crossing substantially at right angles to an electric discharge direction in said electric discharge gate and which connects said electric discharge gate to said discharge wiring layer. However, it is well known in the art to provide an electric charge discharge gate, wiring layer and contact as claimed to allow for the resetting of pixel photodiodes prior to the start of integration to have a consistent base level charge for each picture (Official Notice). Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a discharge gate, wire and contact as claimed to allow for resetting the array.

Allowable Subject Matter

62. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

[claim 20]

63. In regard to claim 20, the prior art does not teach or fairly suggest a solid state imager with a conductive layer intermittently formed above the shift electrode via an insulating layer, a wiring layer formed above the conductive layer via the insulating layer and a contact which is formed into a strip shape along a direction crossing substantially at right angles to the electric charge transfer direction under the shift electrode and which connects the shift electrode to the wiring layer at a gap position of the conductive layer.

Conclusion

64. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art further shows the current state of the art in image sensor wiring configurations and light shielding.

i.	Kawahara et al.	US 4,696,021
ii.	Masatoshi	US 5,028,970
iii.	Negishi et al.	US 5,250,825
iv.	Hatano	US 5,504,355
v.	Nakashiba	US 5,442,396

65. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy J Henn whose telephone number is (703) 305-8327. The examiner can normally be reached on M-F 7:30 AM - 5:00 PM, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R Garber can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJH
3/19/2004

NGOC-YEN VU
PRIMARY EXAMINER